Genesys Logic, Inc.

USB 3.0 Hub Controller

Design Guide

Revision 2.11
Jan. 06, 2015

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Revision History

Revision	Date	Description
1.00	07/15/2010	First formal release
1.10	12/30/2010	Add Ch5 System Design Guideline, p.17~19
1.20	02/22/2011	Add Figure 3.1, p.7 Modify 3.2.8 SS Trace Swap, p.11
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1.40	04/12/2011	Add 3.1.2 2-Layer PCB, p.8 Modify Ch4 The Example of Differential Traces and Impedance, p.18
1.50	04/22/2011	Add Ch6 ESD Protection, p.22
1.60	05/18/2011	Add Figure 5.4 Hub Trace on Mother Board, p.22
1.70	05/19/2011	Update 3.2.8 SS Trace Swap, p.13
1.80	07/08/2011	Add Note for 3.2.8 SS Trace Swap, p.13, 14
1.90	02/02/2012	1.2V DC to DC Converter layout note, p.16 Co-Layout Circuits layout note, p20 GL3521 Circuits layout note, p21
2.00	10/02/2013	Updated CH2 Circuit Design and PCB Layout Guidelines Updated CH3 System Design Guidelines
2.10	01/05/2015	Updated Figure 3.4, p.25
2.11	01/06/2015	Correct page number in 2.10 Revision History

Table of Contents

1. INTRODUCTION

The purpose of this document is to provide suggestions for the design of circuit and PCB layout regarding the USB 3.0 Hub Controllers of Genesys Logic Inc.

2. CIRCUIT DESIGN AND PCB LAYOUT GUIDELINES

2.1 AC Coupling Capacitors

PHY is a component where the transmitter and receiver are located and operated together. The AC coupling capacitors are associated with the transmitter.

Differential Pairs	Capacitor
USB 3.0 SS TX P/N	0.1uF

The AC coupling Capacitor should be placed by closing to Connector. The capacitor body size should be less than or equal to 0603 (**0402 is recommended**). And AC coupling capacitor must be placed symmetrically. (as shown in **Fig. 2.1**)

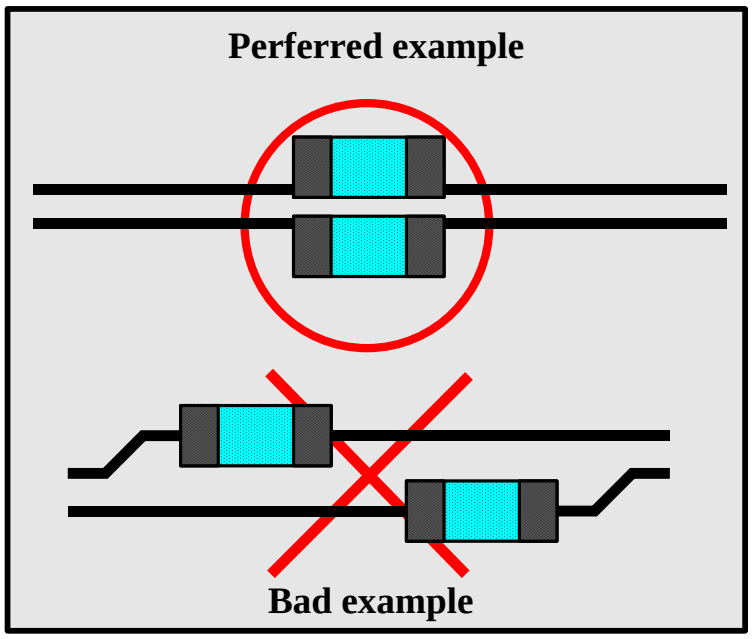


Figure 2.1

2.2 PCB Layer and Material

2.2.1 4-Layer PCB

Four (4) layers and FR4 PCB are recommended to use. Besides, ***the traces of differential signals must be entirely routed over ground plane.***

PCB Layer	Trace Net Name
Top	SS Differential Pair Trace (Hub IC should be placed in the same layer)
Inner 1	GND
Inner 2	POWER,GND
Bottom	HS Difference Pair , Control Signal

2.2.2 2-Layer PCB

PCB Layer	Trace Net Name
Top	SS Differential Pair Trace (Hub IC should be placed in the same layer)
Bottom	HS Difference Pair , Control Signal

2.3 Differential Pairs Trace

2.3.1 Differential Pair Impedance

The differential impedance requirement must be **90 Ohm ± 10 %** and trace width / spacing may be different by PCB material characteristic base on PCB Vendor suggest.

2.3.2 Differential Trace

Keep the trace length of SS TX/RX or HS D+/D- from USB connector to chip as short as possible. And the differential pairs trace routing must be symmetrical. ***USB 3.0 & USB 2.0 differential trace MUST use different layer to avoid cross routing***. Make the differential signal trace GND plane via holes as more as possible to keep GND plane solid with adjacent GND layer.

2.3.3 Differential Trace Length Preliminary Guidelines

Differential Pairs	Signal Referencing	Trace Mismatch Tolerance	Maximum Total Length
USB 3.0 SSTXP/N, SSRXP/N	Ground	≦5mil	9 inches
USB 2.0 DP/DM	Ground	≦50mil	9 inches

2.3.4 Trace Bend

When traces are encountered, please ***use 45° bends*** (or turns) of traces. The inner air gap of a bend, ***A*** should be ***≧ 20 mils*** and the angles between traces should be greater than ***135 degrees. (α ≥ 135°)*** and the length of ***B*** and ***C*** should be ***minimized***.

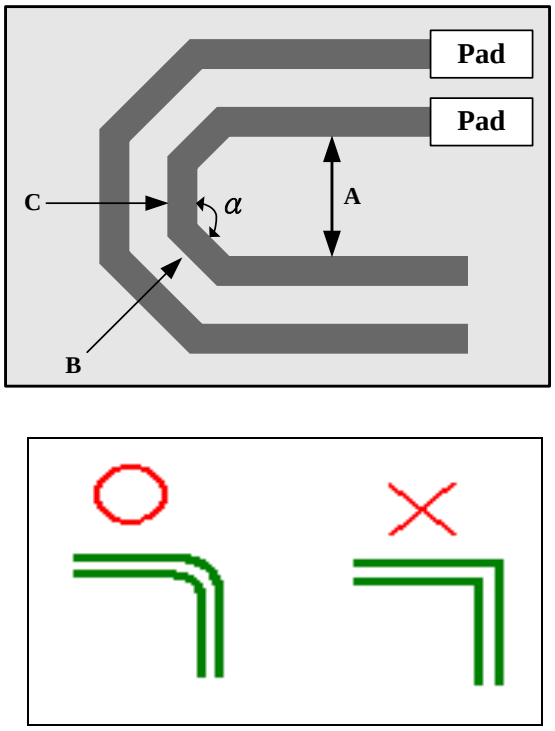


Figure 2.2

2.3.5 Reference Plane

Make sure that the differential trace layer and adjacent layer are with solid GND plane.
The differential pair trace must be ***kept in the outer layer***, and have a ***continual full ground plane*** at ***neighbor layer*** for reference. (See **Fig. 2.3)**

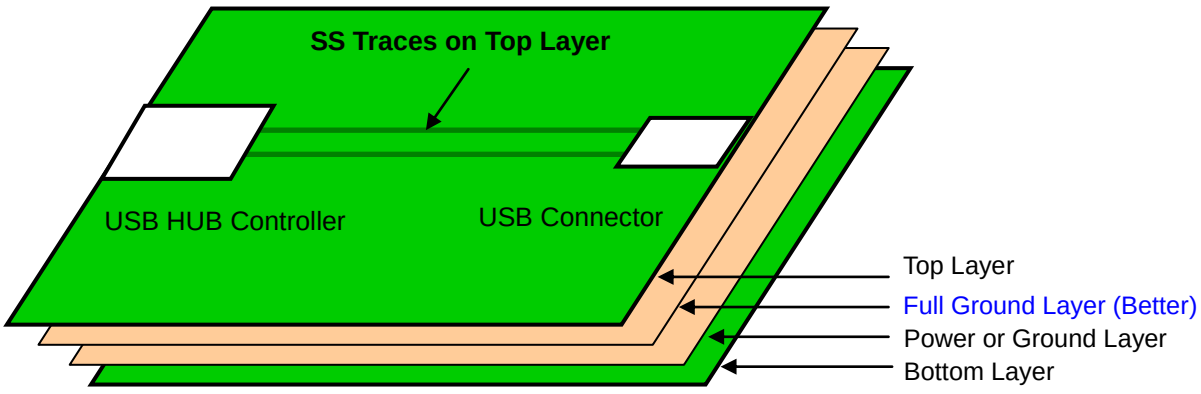


Figure 2.3

A differential pair should ***avoid discontinuation in the reference plane***, such as ***splits*** and ***voids***. When a signal need ***changes layers***, must keep the ***same reference plane*** and the ***ground stitching via*** should be placed by ***closing to the signal via***. A ***minimum of 2 stitching via*** per pair of signals is recommended. Never route a trace so that it straddles a plane split. (See **Fig. 2.4)**

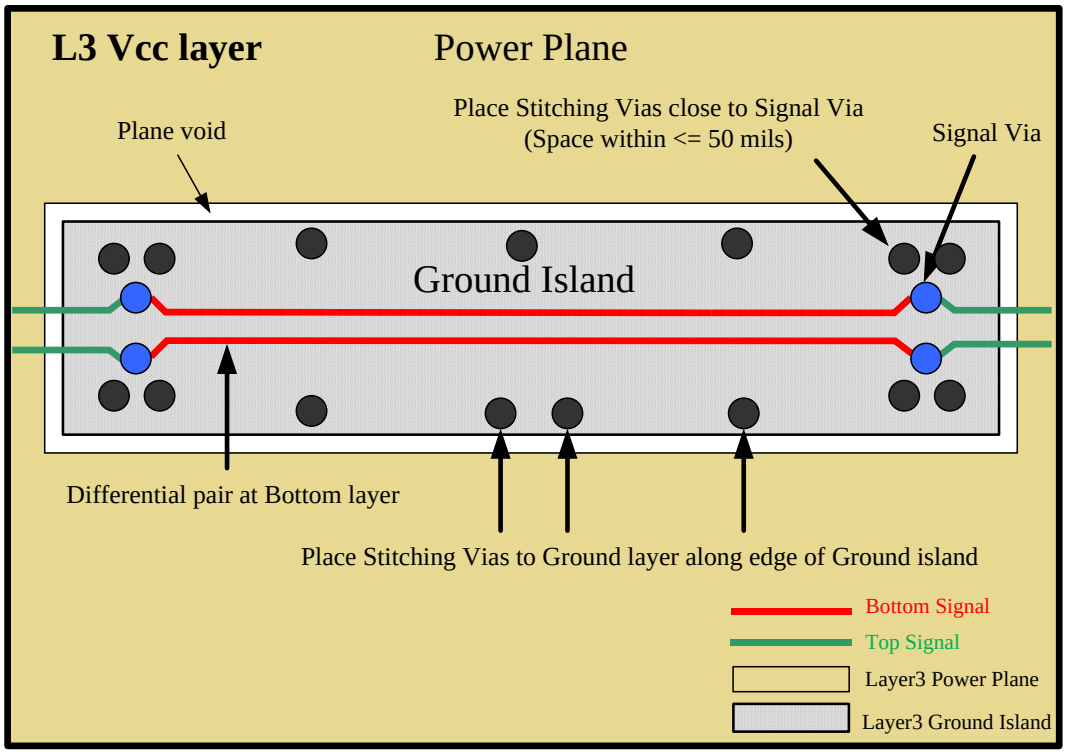


Figure 2.4

2.3.6 Signal Return Path

An incorrect signal return path is one of the most common sources for noise coupling and EMI problems.

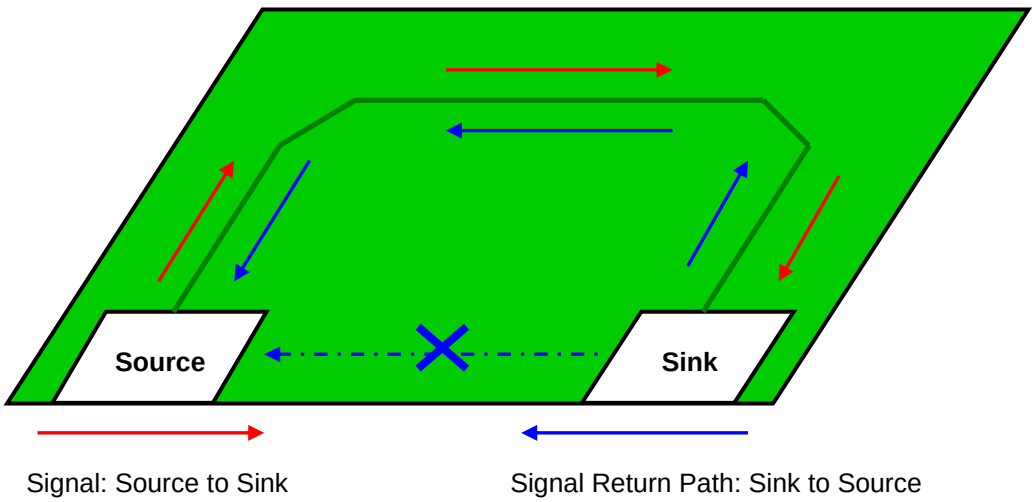
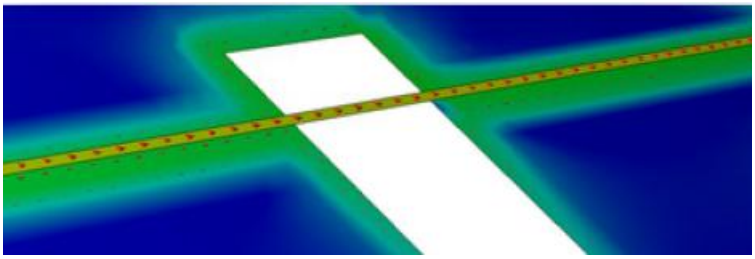


Figure 2.5 Return Current tries to follow the Signal Path

A signal should not be routed over a split plane as the return path is not able to follow the signal trace. If a plane is split between a sink and source, route the signal trace around it. If the forward and return paths of a signal are separated, the area between them acts as a loop antenna.



The Amount of Radiation with Slit （Measurement Result）

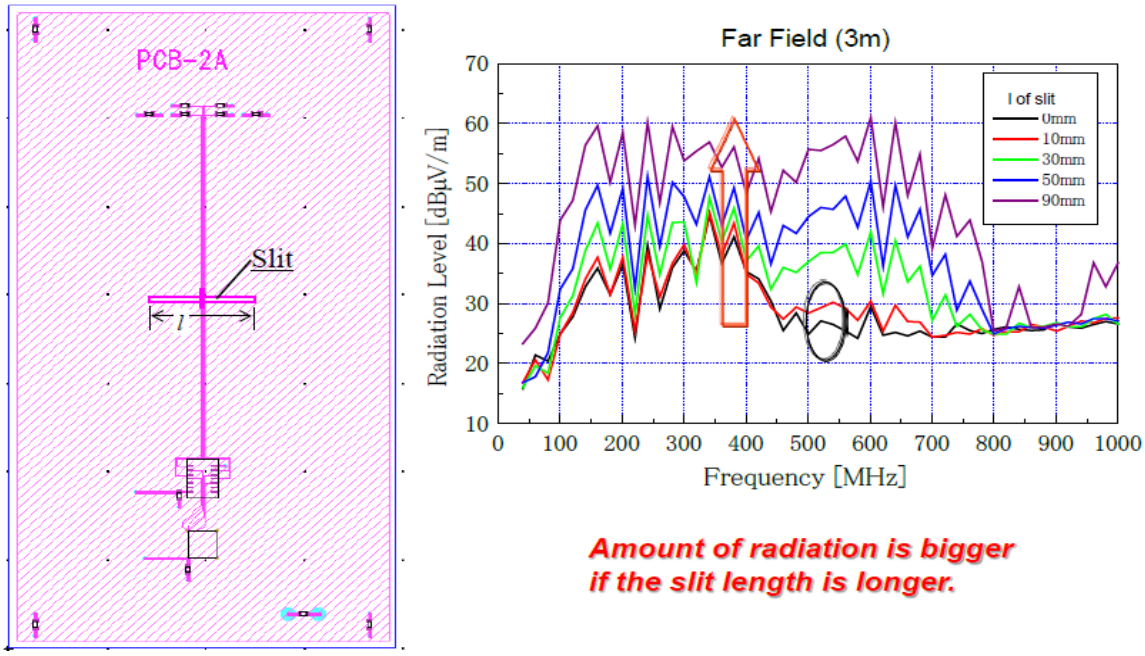


Figure 2.6 Avoid Routing over Split Planes

2.3.7 Differential Pair Layout

The routing of a differential pair must be kept as ***same length***, ***same width***, ***same layer*** and ***fixed space gap***, and also be kept as ***symmetric*** as possible. (as shown in **Fig. 2.7**)

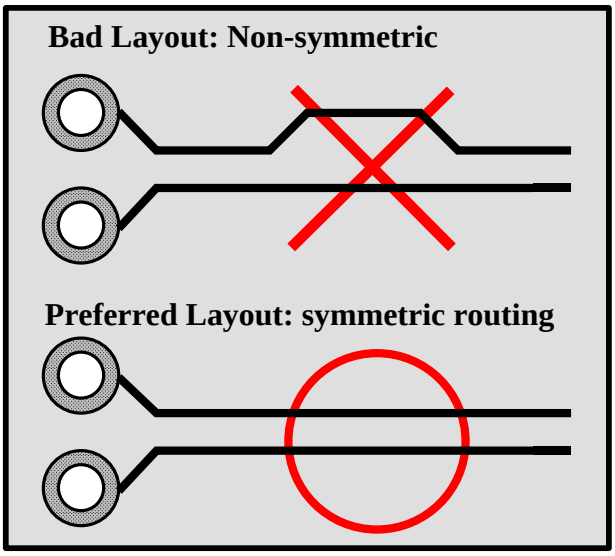


Figure 2.7

When vias are used, they should always be placed in same location and symmetric. (as shown in **Fig. 2.8**)

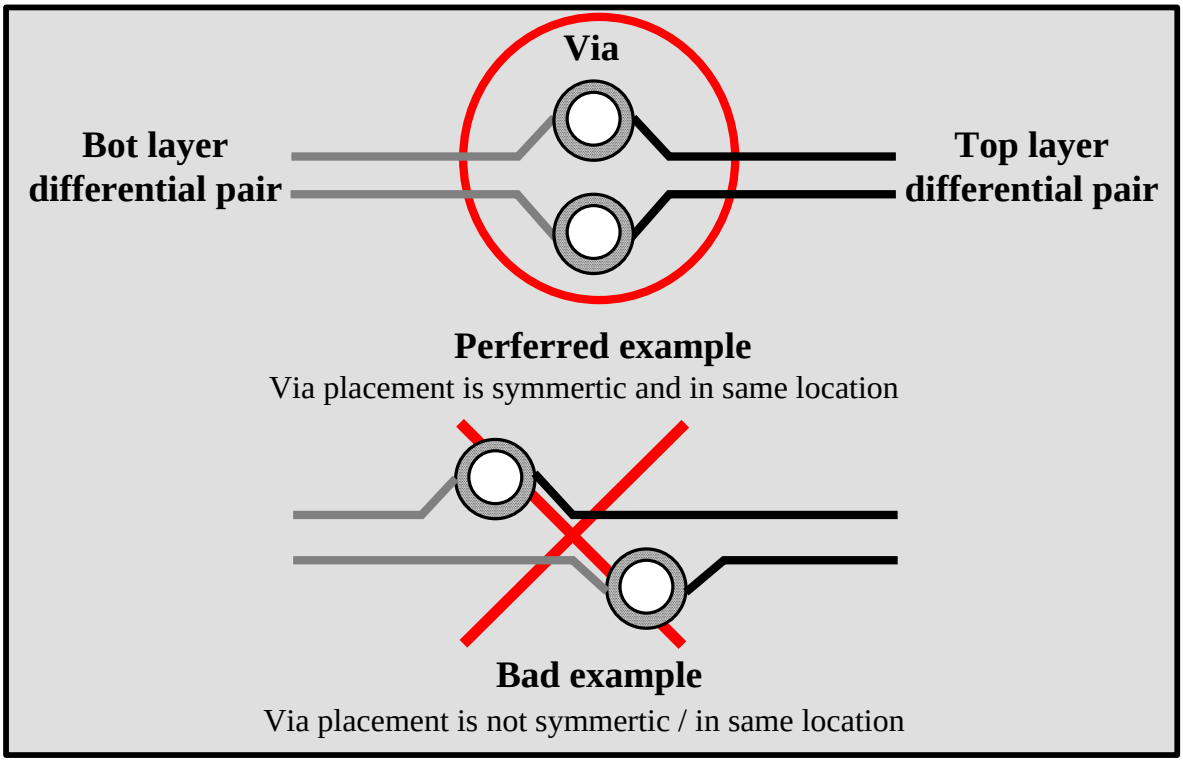


Figure 2.8

2.3.8 Avoid Stub on Differential Traces

Please avoid unexpected stubs. If the Test Pin is needed to be put on the differential pair trace, please make sure there is no stub on any signal trace. (as shown in **Fig. 2.9**)

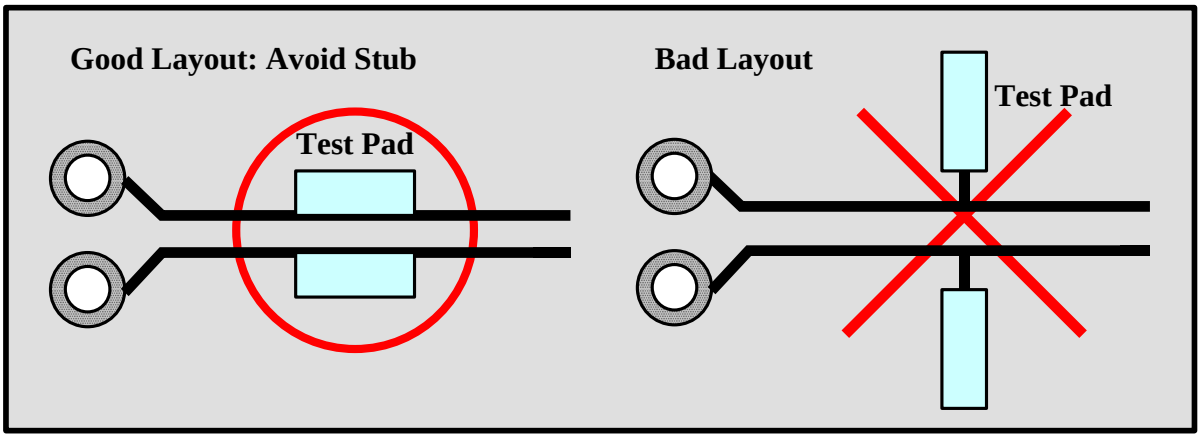


Figure 2.9

2.3.9 SS Trace Swap

If cross trace is needed to make the layout easier, SS differential trace (TXP /TXN or RXP / RXN) N&P can be swapped. As shown in **Fig 2.10**

- Pin TXN of the IC can be connected to TXP of the connector.
- Pin TXP of the IC can be connected to TXN of the connector.
- Pin RXN of the IC can be connected to RXP of the connector.
- Pin RXP of the IC can be connected to RXN of the connector.

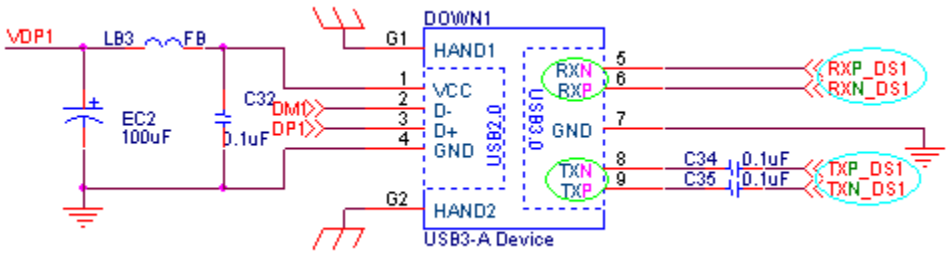


Figure 2.10

Note:

1. Because some devices may not support RXN/RXP swap function, it is **NOT** recommended swap Hub TXN and TXP traces for better compatibility.
2. If TXN and TXP swap function is needed for layout concern, Hub firmware needs to be modified accordingly. The "TXP/N Swap" function **MUST** be selected in Configuration of the Genesys Logic USB 3.0 Hub FW ISP Tool at the same time. Choose the port whose TXN and TXP traces is swapped. (as shown in **Fig 2.11**)

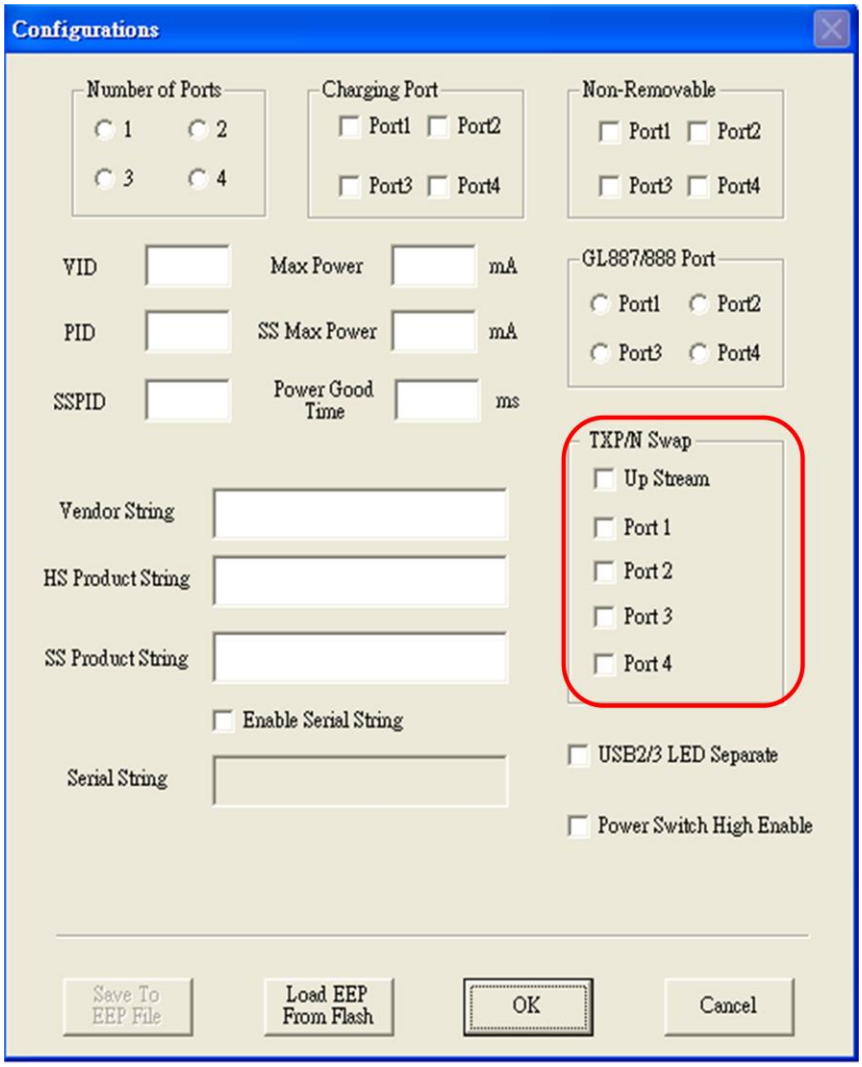


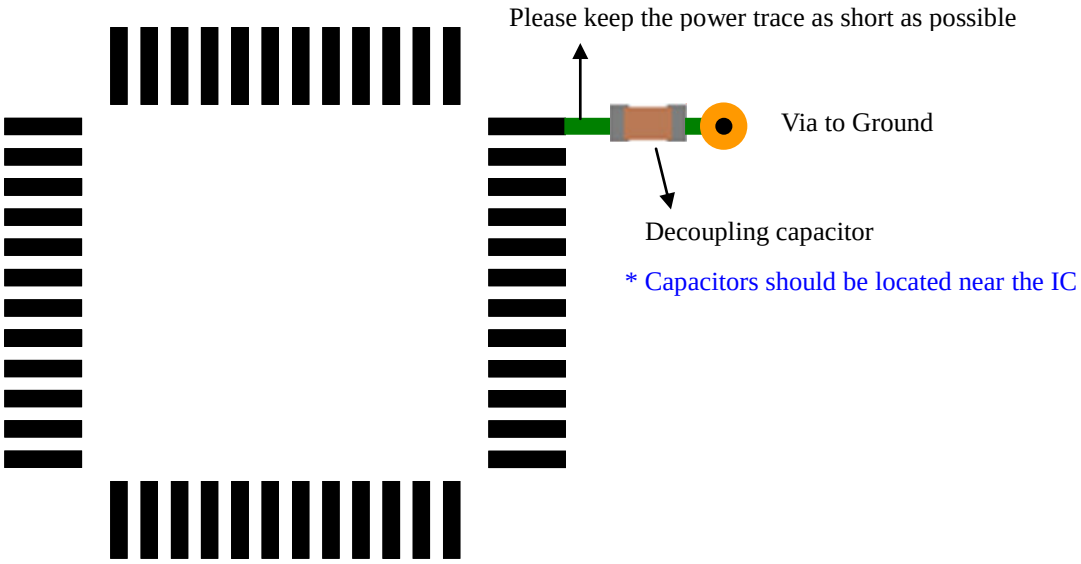
Figure 2.11

2.4 Circuit and Component Placement

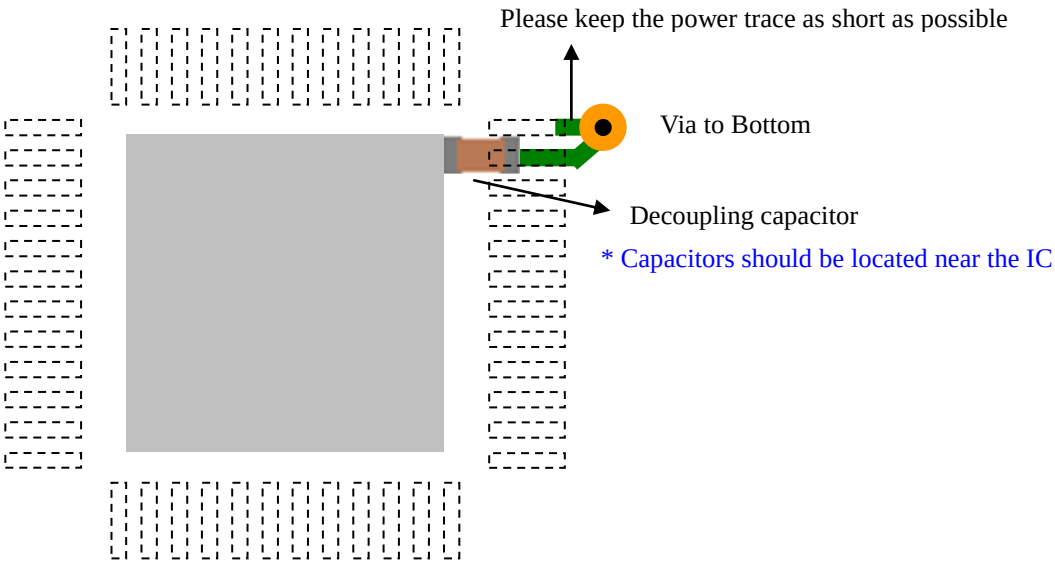
2.4.1 Decoupling Capacitors

Please place the 0.1uF decoupling capacitor as close the UBS 3.0 Hub power pins as possible.

An example of decoupling capacitor positioning on top layer:



An example of decoupling capacitor positioning on Bottom layer:



2.4.2 RTERM Resistor

RTERM reference resistor use 680 ohm ±1% and place as close to the IC as possible.

2.4.3 Crystal Circuit

1. 50ppm precision class is recommended for the X'tal.

2. Keep the distance between crystal and the IC less than 1cm to avoid triggering high frequency oscillation on PCB. If over 1cm is unavoidable in the design, place the capacitors and the resistor as close as possible to the IC. Recommend less than 1cm if possible. And the resistor need be between the IC and the capacitor. See **Fig. 2.12**

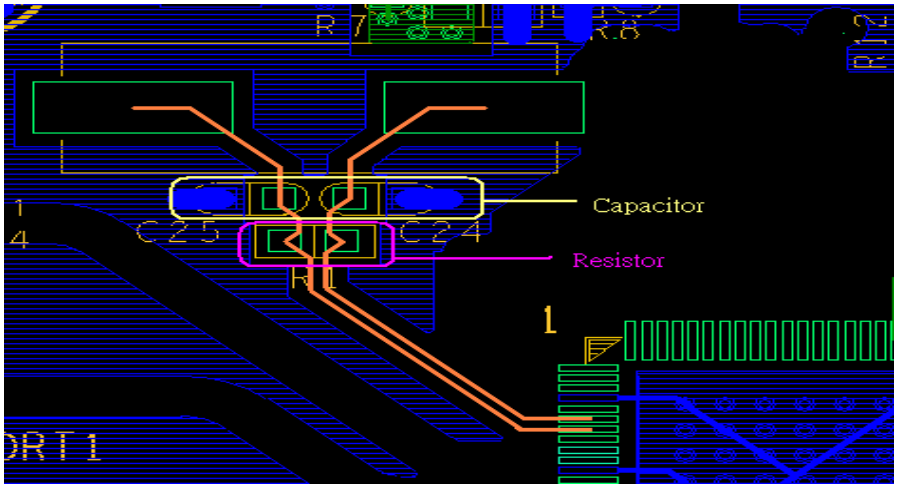


Figure 2.12

3. Do not route X1 and X2 underneath the IC. In this case, it may cause noise on PCB and will trigger high frequency oscillation.

4. The crystal traces shall be symmetrical and parallel in order to get better oscillation wave form and better EMI protection (as shown in **Fig. 2.13**).

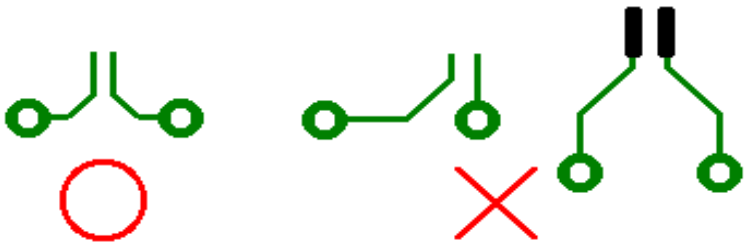


Figure 2.13

2.4.4 Reset Circuit

Keep the Reset circuit placement as close to the IC as possible.

2.5 Power Source

Make sure that the DC to DC converter output voltage is 1.2V. Follow the PCB layout guidelines for optimal performance of UP1722PDE6.

1. For the main current paths, keep their traces short, direct and wide.
2. Put the input/output capacitors as close as possible to the device pins.
3. LX node is with high frequency voltage swing and should be kept in small area. Keep analog components away from LX node to prevent stray capacitive noise pick-up.
4. Keep the connect feedback network behind the output capacitors. Place the feedback components near the UP1722PDE6 and keep the loop area small. .
5. A ground plane is preferred, but if not available, keep the signal and power grounds segregated with small signal components returning to the GND pin at one point. They should not share the high current path of C_{IN} or C_{OUT}.
6. Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. These copper areas should be connected to VIN or GND.

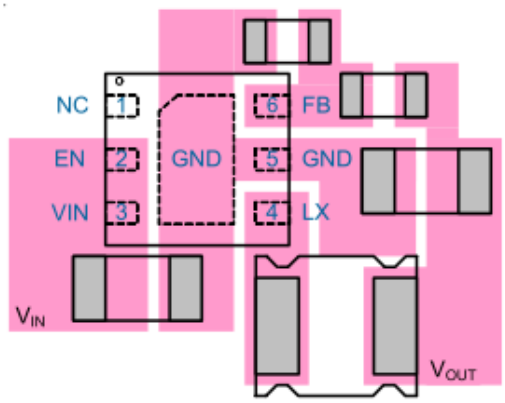


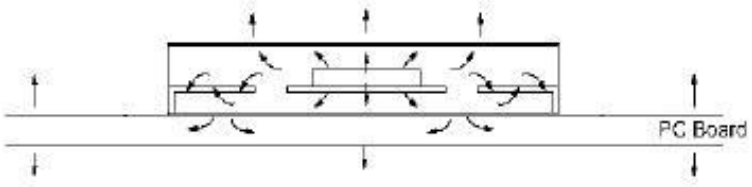
Figure 2.14

2.6 Power Trace of Charging Downstream Port

USB3.0 Hub allows BC1.2 portable device draw 1.5A from each charging downstream ports (CDP) by compliant with USB Battery Charging Specification rev1.1, so ***the width of charging downstream port VBUS trace is better to > 60mils*** to support enough current to avoid voltage drop**.** And the total adapter or system power source should also consider how many CDPs support to provide enough current for fast charging. For example, if the design supports four charging downstream ports, the 5V power supply must be capable of delivering total 6Amps.

2.7 Thermal Reduction

Optimum layout suggestion for thermal sensitive design: The copper under chip GND area is through via holes and inner 2 (GND layer) to reach heat sink effect.

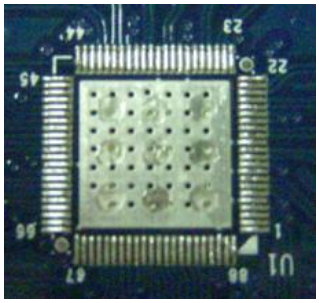


The two paths of heat dissipation shown in the above figure are as follows:

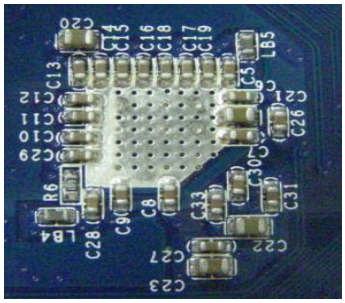
1. IC chip → Package → Atmosphere
2. IC chip → Package → lead → PC board → Atmosphere

Figure 2.15

To prevent temperature surge on silicon surface under worst environment, it is strong recommended to use following layout option to increase the efficiency of silicon heat spreading. The copper under chip GND area must be appeared on bottom layer and drill more through holes (0.5mm) to reduce chip thermal impact.



Top View



Bottom View

Chip ground VIA

Diameter ─ 0.5mm

VIA to VIA gap ─ 50 mil

2.8 Trace Width and Adjacent Space Gap

2.8.1 USB 3.0

The edge-to-edge spacing of adjacent pairs should be greater than 20 mils at least. The differential pair traces should be kept at least 20 mils away from the edge of the Power or GND plane (trace), signal trace and vias.

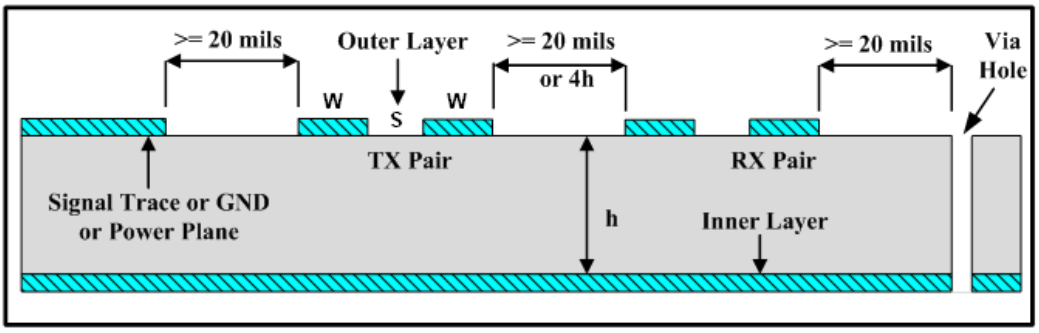


Figure 2.16

*Note: Different Port differential signal trace Gap ≥20 mils or use GND plane isolate, The GND plane and differential signal trace Gap ≥20 mils.

2.8.2 USB 2.0

The GND of the signal lines shall have spacing of at least 20mil with the signal lines.

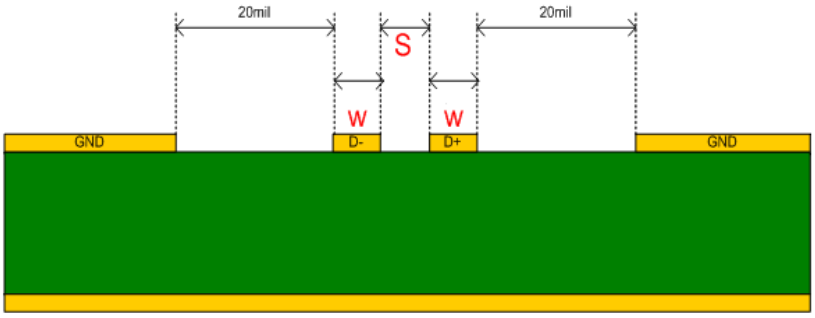


Figure 2.17

2.8.3 Recommend Width and Space for USB 2.0 & USB3.0 Trace

Please refer to the following table for the recommending width and spacing on 4-layer PCB setting:

*Note: The trace width (W) / spacing (S) may be different by PCB material characteristic base on PCB Vendor suggest.

Differential Pair	Setting 1	Setting 2
Trace width (W)	6mil	8mil
Intra pair spacing (S)	6mil	7mil
Target impedance	90 Ohm ± 10 %	

2.9 GL3520/GL3521 Co-Layout Notice

1. The layout trace diagram of 1.2V DC/DC converter is described as **Fig. 2.18**. Please route the UP1722PDE6 power trace first, and then place GPIO (PAMBER#). The width of SW 1.2V power trace line is recommended to be 40 mils. The trace of FB is recommended to be as short as possible, and not to be routed through the layer of EMI protection. There is large current passing though the pin 2 of UP1722PDE6. This pin has to be connected with the ground of C_{IN} and C_{OUT}, and the trace has to be wide. Increase the amount of via holes at the ground of pin 2. Increase via holes at the ground connected with C_{IN}, C_{OUT}, and the pin 2 of UP1722PDE6, and widen the trace. Please also refer to Section 3.4 Power Source for more information.
2. The layout trace diagram of 1.2V or 3.3V power trace is described as **Fig. 2.19**. Please route the power trace first, and then place GPIO (PAMBER#). The width of DVDD12 power trace line is recommended to be 40 mils, and the width of DVDD33 power trace line is to be 30 mils.

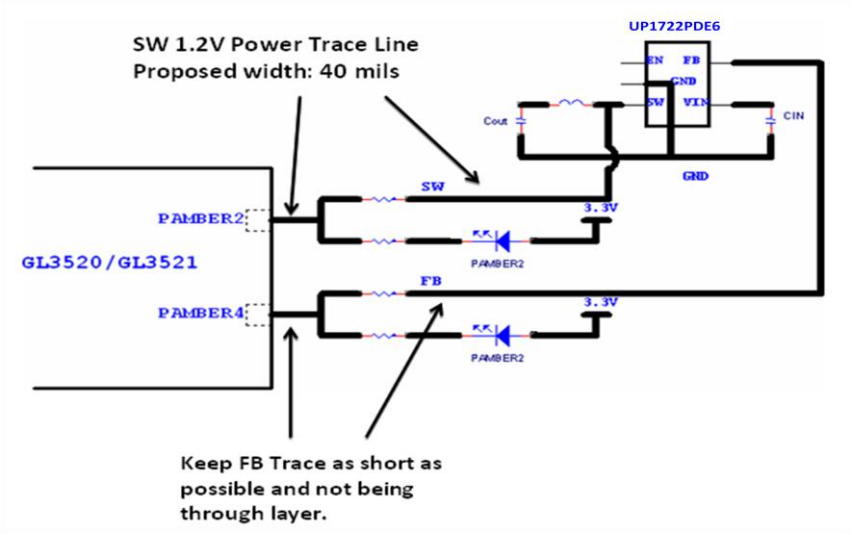


Figure 2.18

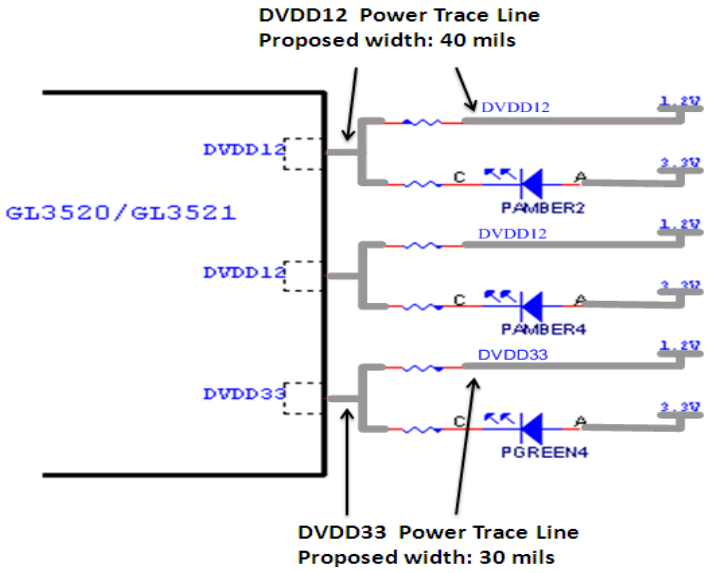


Figure 2.19

2.10 GL3521 Layout Notice

1. The layout trace diagram of 1.2V power is described as **Fig. 2.20**. The width of SW 1.2V power trace line is recommended to be 40 mils. The trace of FB is recommended to be as short as possible, and not to be routed through the layer of EMI protection. Please also refer to Section 3.4 Power Source for more information. The resistor divider R1 and R2 must be connected between the (+) plate of C_{OUT} and a ground line terminated near GND. The SW should be connected to inductor by wide and short trace, and keep sensitive components away from this trace. There is large current passing though the pin 88 GND of GL3521. This pin has to be connected with the ground of C_{IN} and C_{OUT}, and the trace has to be wide. Increase the amount of via holes at the ground of pin 88. Increase via holes at the ground of C_{IN} and C_{OUT}

2. The layout trace diagram of 1.2V or 3.3V power trace is described as **Fig. 2.21**. The width of DVDD12 power trace line is recommended to be 40 mils, and the width of DVDD33 power trace line is to be 30 mils.

3. Please reduce at least 2 vias when the 5V or 12V power trace is needed to go through different layers. Please refer to the **Fig. 2.22** for more detailed information.

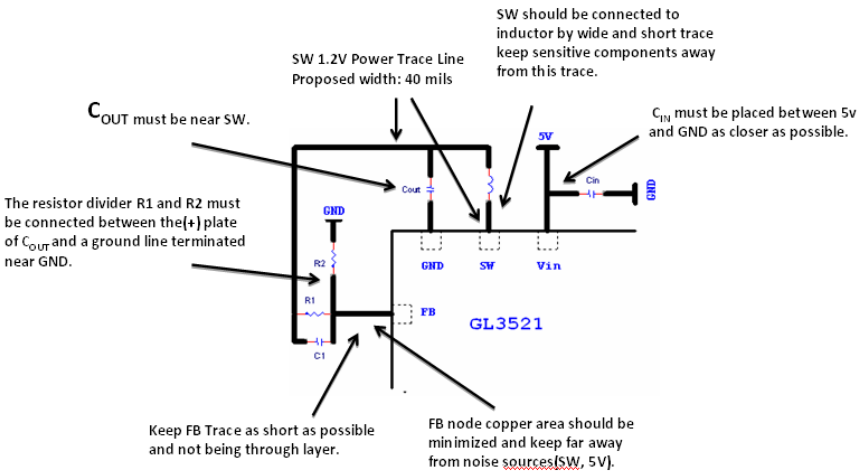


Figure 2.20

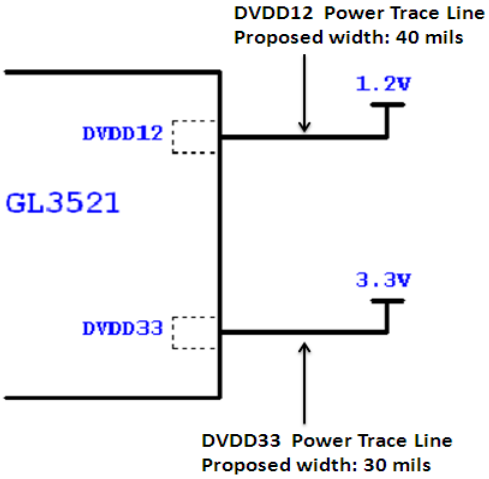


Figure 2.21

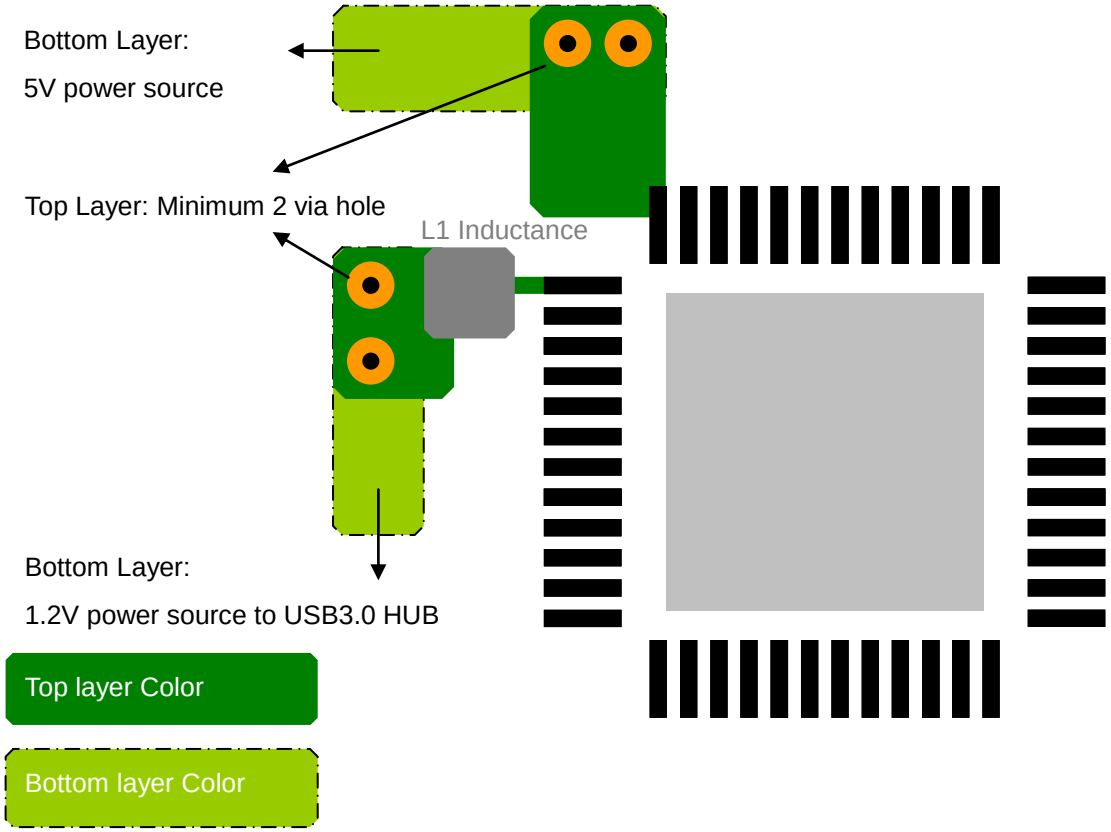


Figure 2.22

3. SYSTEM DESIGN GUIDELINES

3.1 System Design Overview

In order to cover the wide range of expected application, two compliance channels are defined for electric compliance testing. And, these two compliance channels (back channel and front channel) are used to check the channel loss and reflection effect of Device or Upstream port of HUB. The figure below shows the compliance channel designs for hosts, devices and cables. The host and cable compliance channels are used in testing of device/HUB (UP) designs. The device and cable compliance channels are used for testing of host/HUB (DP) designs.

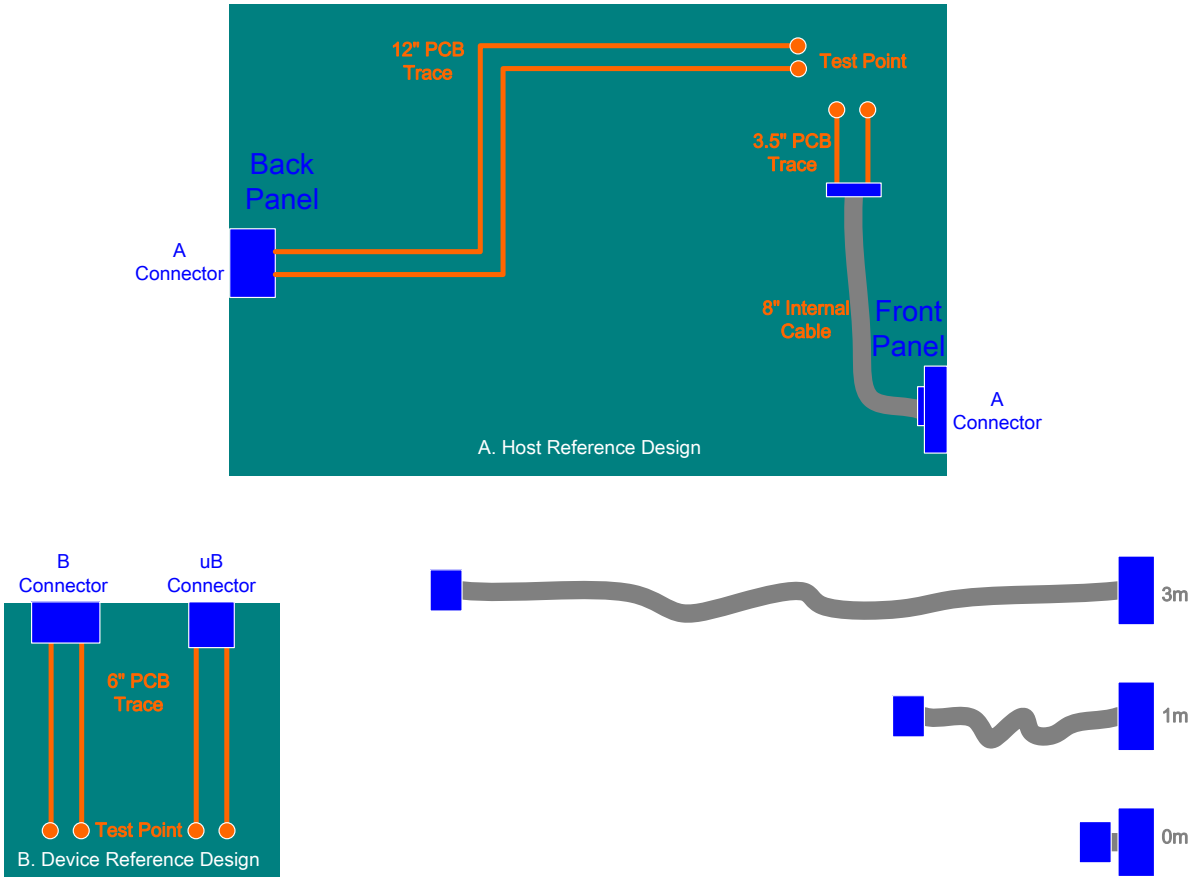


Figure 3.1 Compliance Channel

3.2 Channel Description – with a Cable

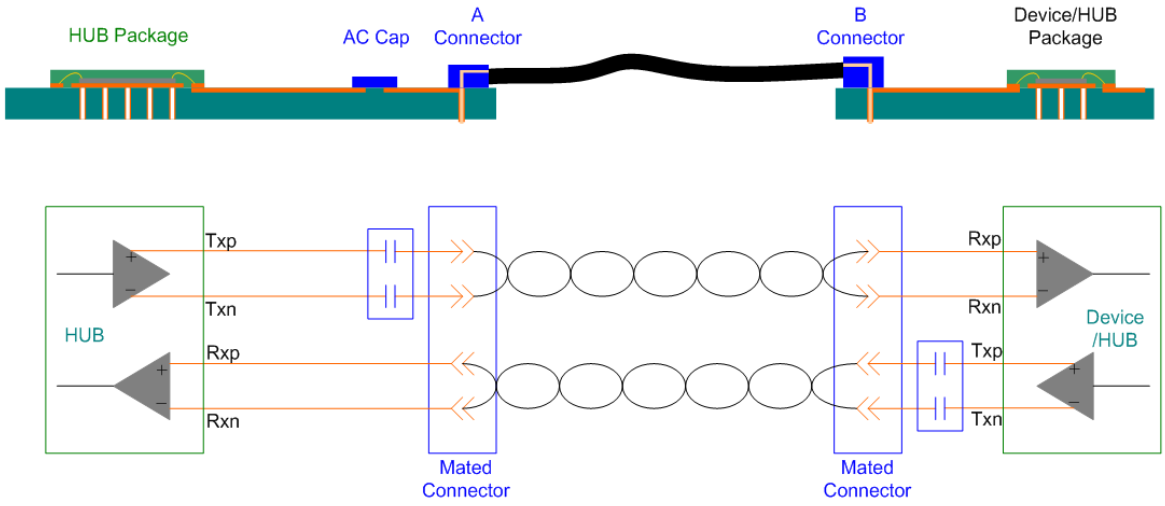


Figure 3.2 Channel Model with a Cable

Fig. 3.2 shows the channel topology (with a cable). The insertion loss of 8/7/8 FR4 trace is around 0.296dB per inch (2.5G signal & PCB trace w/o via). The insertion loss of 34AWG cable is around 4.4dB per meter. So, the worst case of total insertion loss is around -20dB (It is equal to 9-inch (-2.664dB) + 3m (-13.2dB) + 6-inch (-1.776dB) + -2dB (-1dB/mated connectors)), and also need to take care about crosstalk (NEXT, FEXT). Finally, the HUB PCB design must pass compliance channel testing.

3.3 Channel Description – without a Cable

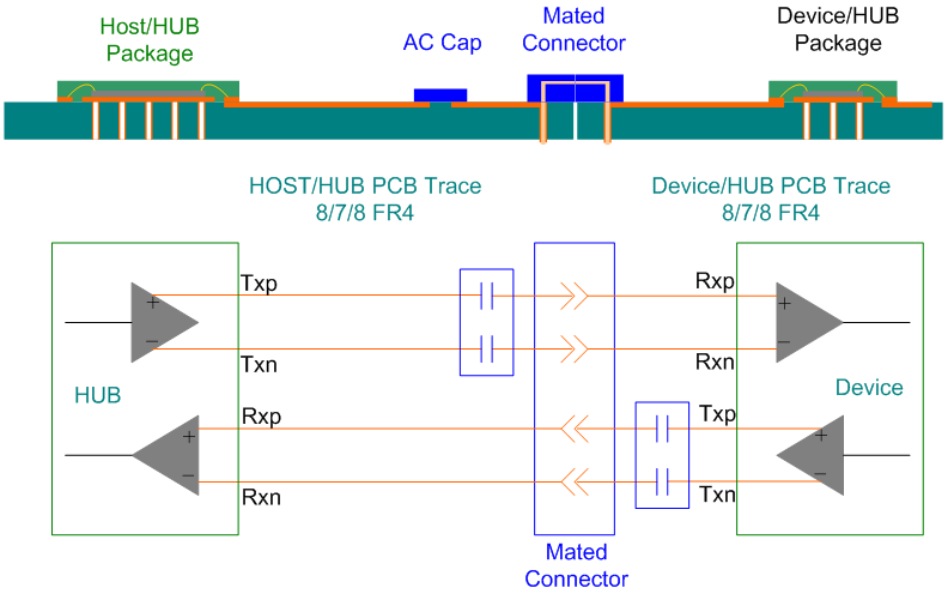


Figure 3.3 Channel Model without a Cable

Fig. 3.3 shows the channel topology (without a cable). The insertion loss of 8/7/8 FR4 trace is around 0.296dB per inch (2.5G signal & PCB trace w/o via). Based on the previous case description, the max insertion loss is 20dB (including PCB trace, PCB via and connector). However, as described in the first section, the performance is determined by channel loss, reflection, crosstalk, and the most of reflection and crosstalk are caused by connector design. So, keeping 9 -inch and 6-inch FR4 trace length can gain much margin.

3.4 Hub Trace on Mother Board

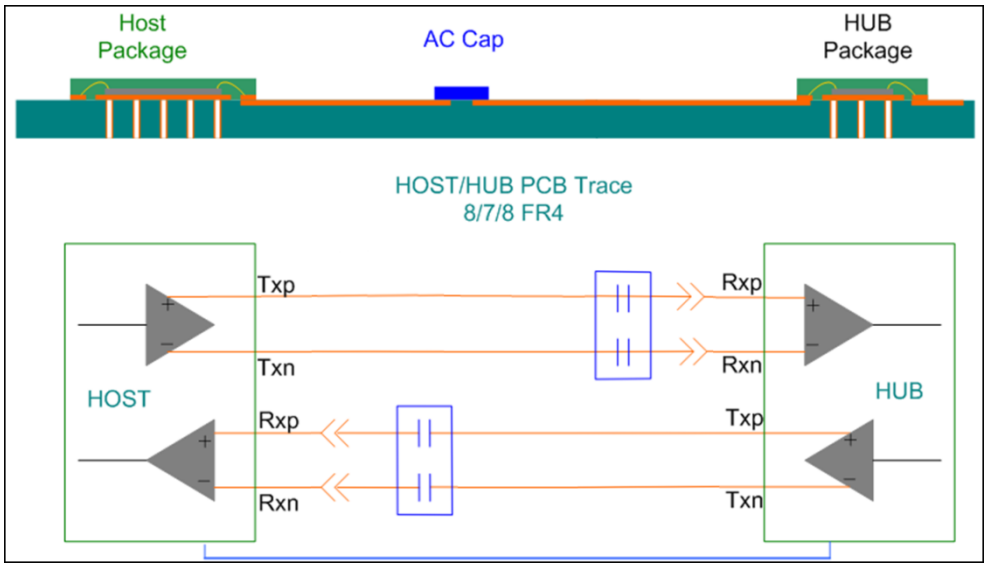


Figure 3.4 Hub Upstream Port Connected to Host

Fig. 3.4 The recommended length of Hub trace is up to 9 -inch on the mother board. However, if the Host trace length is less than 9- inch, use the shorter one of these two numbers.

4. ESD PROTECTION

4.1 Hub

It is suggested to add ESD protection component (ex. TVS) between the connector and IC to provide better ESD protection. (as shown in **Fig. 4.1**)

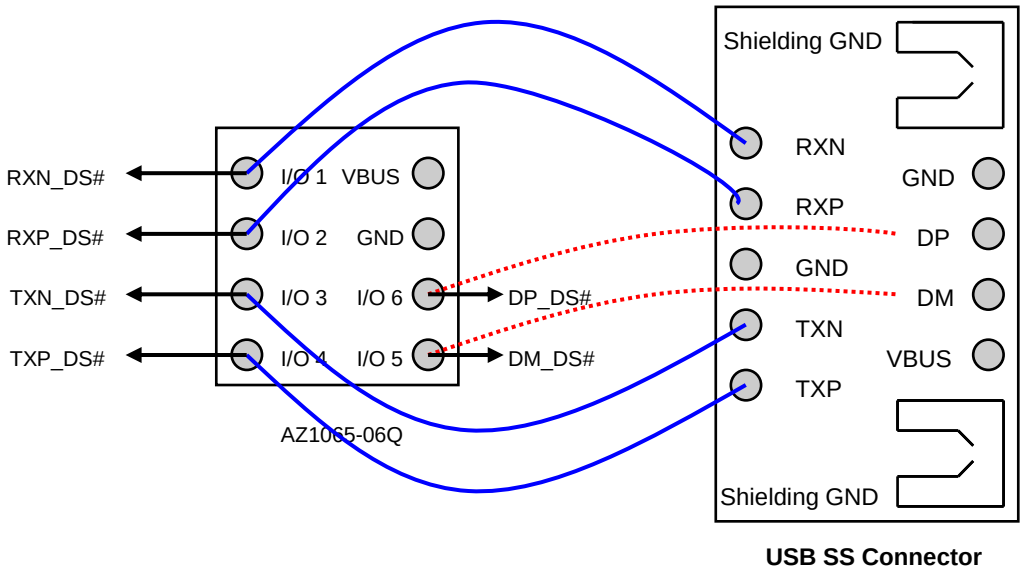


Figure 4.1

4.2 Hub with External Charger IC

Fig. 4.2 shows the suggested layout guide if the external charger IC is implemented for battery charging function.

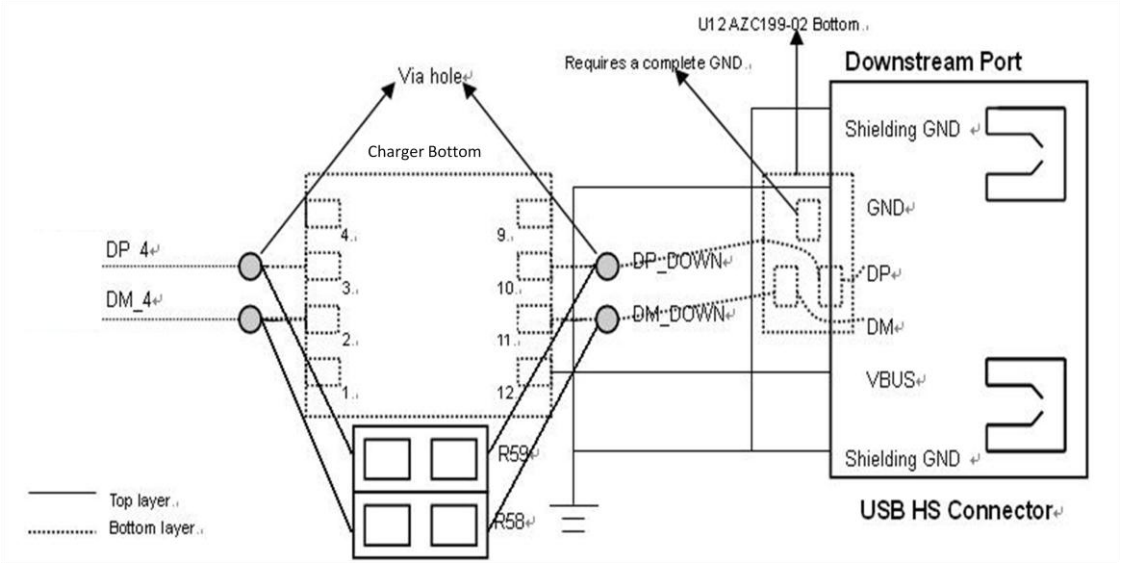


Figure 4.2